THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

This opinion (1) was not written for publication and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RODNEY A. MATTISON

Appeal No. 95-2218
Application 07/902,073

ON BRIEF

Before THOMAS, HAIRSTON, and TORCZON, Administrative Patent Judges.

TORCZON, Administrative Patent Judge.

FINDINGS OF FACT AND CONCLUSIONS OF LAW

FINDINGS OF FACT

We have reviewed the record in its entirety in light of the arguments of Appellant and the examiner. Our decision presumes familiarity with the entire record. A preponderance of the evidence of record supports each of the following fact findings.

A. The nature of the case

1. This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 12-17. (Paper 13.) Appellant has canceled claims 1-11 and 18. (Paper 8 at 2.) The examiner has allowed claims 19-29. (Paper 9 at 1.) We reverse the rejection of

claims 13 and 14 and enter a new ground of rejection for the remaining claims.

2. Appellant filed the subject application on 22 June 1992. He claims no priority under 35 U.S.C. §§ 119 or 120.

3. The subject matter of the invention is a delayed read data single shot (DRDSS) circuit for delaying a data signal read from different zones on a zone-bit-recorded (ZBR) data storage device. (Paper 1 at 1.)

4. Claim 12, the only independent claim on appeal, sets forth the subject matter of the invention as follows:

> Window margining apparatus for detecting the occurrence of a data pulse reproduced from a zone bit recorded data storage device within a window duration, comprising:
> a delayed read data single shot (DRDSS) circuit for delaying by an adjustable amount the data pulse reproduced from said data storage device to produce a DRDSS-delayed data pulse, the amount of delay being determined by the zone from which said data pulse is reproduced;
> variable delay means coupled in common with said DRDSS circuit for delaying said data pulse reproduced from said data storage device;
> window pulse generating means coupled to said DRDSS circuit for generating a window pulse of predetermined duration in response to the DRDSS-delayed data pulse; and
> detecting means coupled to said window pulse generating means and to said variable delay means for detecting if the data pulse delayed by said variable delay means occurs within said window pulse.

5. According to the disclosure, "the delay circuit . . . has been described by those of ordinary skill in the art as a

one-half cell delay, an anticipator, a variable bit cell delay, a one-third cell delay and a delayed read data single shot (DRDSS). (Paper 1 at 3, emphasis added.)

6. The window pulse generating means may comprise "a phase-locked loop synchronized with said DRDSS-delayed data pulse". (Claim 16, which depends from claim 12.) The disclosed window generator "may comprise the phase locked loop included in data separator 20". (Paper 1 at 28.) "The phase locked loop is shown as a conventional PLL comprised of [voltage-controlled oscillator] VCO 30, a frequency divider 32, a comparator 34, a charge pump 38 and a filter 40, all interconnected in a loop." (Paper 1 at 12.) "Microprocessor 42 is coupled to VCO 30 and is adapted to supply a zone identifying signal to the VCO which acts as a 'course' control." (Paper 1 at 13.)

B. The rejection

7. The examiner has rejected (Paper 9 at 3) claims 12-17 under 35 U.S.C. § 103 in view of:

Pederson	5,109,304	28 Apr. 1992
Fischler et al. (Fischler)	4,894,734	16 Jan. 1990

8. Claim 17 also stands rejected (Paper 9 at 6) under 35 U.S.C. § 103 in view of Pederson, Fischler, and

Tanaka et al. (Tanaka)	5,142,420	25 Aug. 1992 (filed 23 Apr. 1990)

9. The Pederson reference teaches a window margining method and apparatus for detecting defects on a hard disk. (1:7-14.) Pederson lists many compelling reasons why a hard disk designer would want a window margining defect detection system. (1:15-3:34.) Pederson does not teach zone bit recording or the circuitry needed for it, but none of Pederson's reasons for having error-detection circuitry are unique to Pederson's disclosed constant bit rate recorded hard disk system.

10. For the purposes of appeal, Appellant has conceded that "Pederson's variable delay 22, window generator 26 and error detector 32 . . . correspond[] to Appellant's claimed 'variable delay means,' 'window pulse generating means' and 'detecting means[]'", respectively. (Paper 14 at 9.) Appellant further concedes that "Pederson's error detector 32 corresponds to the claimed 'first comparator means[]'". (Paper 14 at 27.) The examiner concedes that "Pederson does not have an element similar to the DRDSS circuit." (Paper 9 at 4.) We find these concessions to be consistent with the record.

11. Pederson's variable delay circuit **22** and window generator **26** are coupled in common to the CLOCK signal. (7:37-8:15; Fig. 2.) Pederson's error detector **32** is coupled to the window generator **32** and (via multiplexer **28**) to the variable delay **22**. (7:29-65; Fig. 2.) The window generator **26** includes a

phase-locked loop (PLL) synchronized with the clock signal. (7:37-46.)

12. Pederson does not teach three separate comparators comparing the output of the variable-delayed data pulse and the window pulse, the DRDSS-delayed data pulse and the window pulse, and the outputs of the preceding comparators, respectively, as set forth in claim 13.

13. The Fischler reference teaches a method and apparatus for constant density recording of zones on a hard disk drive. (2:12-29.) Fischler teaches that constant-density recording has the advantage of maximizing disk storage capacity. (1:23-41.) Fischler's zone-based constant-density recording system is disclosed to be a good compromise of access time, cost, size, reliability, and storage capacity. (1:42-2:29.)

14. Appellant concedes that a hard drive using Fischler's constant density recording is the same as the claimed "zone bit recorded data storage device". (Paper 14 at 9.) Appellant further concedes for the purposes of appeal "that Fischler's anticipator [**62**] corresponds to Appellant's DRDSS circuit." (Paper 14 at 10.) We find these concessions to be consistent with the record.[1]

[1] Appellant's disclosure could be read to discourage the use of Fischler's anticipator because, among other things, it (continued...)

15. Fischler discloses (9:11-10:14) a variable frequency oscillator (VFO) **12** that "is used to establish a decode window to separate the data from the read channel." (9:45-46.) The VFO includes an anticipator **62** (9:11-13) and a voltage control oscillator (VCO) **65** (9:35-37; Fig. 3). The VFO is a PLL (9:59-60), the phase of which is controlled by the anticipator (9:49-53).

16. Fischler's PLL (Fig. 3) appears to be structurally equivalent to the "conventional" PLL that comprises Appellant's window generator. Fischler's PLL has a VCO **65**, a frequency divider **68**, a comparator (dual-mode phase-frequency detector **63**), a charge pump **64**, and a filter **77**, connected in a loop. (Fig. 3.) The output of filter **77** is the fine control signal. (9:28-30.) The comparator also receives a reference signal FREF (via anticipator **62**) from a reference oscillator (VCO **86**) except during read operations. (8:61-9:19.) Fischler provides coarse

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[1](...continued)
takes up too much "real estate". (Paper 1 at 4-5.) Nevertheless, Appellant has not drafted his claim so as to exclude Fischler's anticipator. In re Morris, __ F.3d ___, ___, 43 USPQ2d 1753, 1759 (Fed. Cir. 1997) (Applicants bear the burden of precisely claiming their inventions.). For instance, Appellant did not use means-plus-function language to claim the DRDSS circuit. Cf. Greenberg v. Ethicon Endo-Surgery Inc., 91 F.3d 1580, 1584, 39 USPQ2d 1783, 1786 (Fed. Cir. 1996). Moreover, Appellant has conceded the equivalence of Fischler's anticipator to the claimed DRDSS circuit for the purposes of appeal.

control signal **80** based on zone control signal **18** via digital-to-analog converter **67**, which is coupled to the VCO **65**. (9:30-34.)

17. Although Appellant characterizes the VFO description as "less than clear" (Paper 14 at 10), we presume Fischler's disclosure to be adequate for the purposes of an obviousness rejection absent evidence to the contrary. In re Epstein, 32 F.3d 1559, 1568-69, 31 USPQ2d 1817, 1823-24 (Fed. Cir. 1994). Appellant has not offered evidence that Fischler's disclosure is not enabling.

18. Fischler does not disclose a window-margining defect-detection apparatus or method. One consequence of this is that Fischler does not teach three comparators in a defect-detecting means.

19. The Tanaka reference, Appellant argues, adds nothing to the teachings of Fischler. (Paper 14 at 6 n.3.) The examiner's answer neither responds to this point nor offers any further discussion of Tanaka. Since we do not see any basis for relying on Tanaka beyond the teaching of a VCO, which is already taught in Fischler, we find Tanaka to be cumulative to Fischler for the purposes of rejecting claim 17.

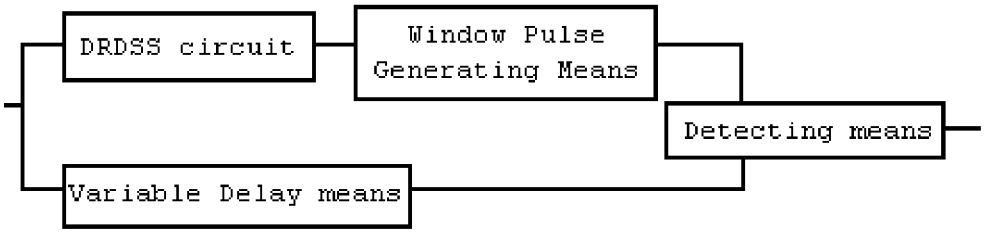
20. We rely on the references to show the level of skill in the art. In re GPAC, 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995).

21. Appellant has not presented objective evidence of secondary considerations for us to review. Cf. In re Geisler, 116 F.3d 1465, 1470, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997) (Such evidence should be in the specification or other evidentiary submission.).

CONCLUSIONS OF LAW

A. Claim interpretation

1. During examination, we must give claims their broadest reasonable interpretation since Applicants are in the position to amend their claims to avoid problems. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Applicants are obliged to claim precisely. Morris, F.3d at ___, 43 USPQ2d at 1759. When appellants concede for the purposes of appeal that an elements in their claims cover prior art structures, we must take such concessions at face value unless the concessions are manifestly unreasonable. Stripped to its essentials, claim 12 (as argued) requires the following elements arranged as shown and no more:



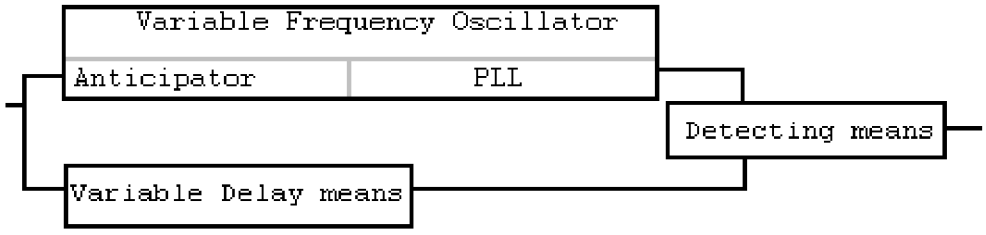
B. Claims 12 and 15-17 are obvious

2. We agree with Appellant's complaint that the examiner's combination of Pederson and Fischler appears to be the product of hindsight. (Paper 14 at, e.g., 15.) The examiner looks to Fischler to supply an element missing from Pederson in order to meet the claimed invention. (Paper 9 at 4-5.) While it is true that hindsight is necessary to the extent of narrowing the focus of the examination to the claimed subject matter, the motivation to combine must make sense in terms of the prior art per se without reference to the claims. In re McLaughlin, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971). Although the examiner was generally on the right track, we conclude that his rationale was unacceptably based on hindsight.

3. We, nevertheless, conclude that the subject matter of claims 12 and 15-17 would have been obvious in light of Pederson and Fischler. The Fischler reference would have motivated a person having ordinary skill in the art to use a zone bit recorded (ZBR) hard disk system like Fischler's for the reasons (access time, data density, cost, reliability, size) Fischler discloses. Findings 13 and 14, supra. The same person would also have been motivated to provide hard disk diagnostic circuitry for a ZBR system for the same reasons (many sources of defects that can occur after the disk is in use) Pederson

discloses. Finding 9, supra. Thus, on reading Fischler and Pederson, a person having ordinary skill in the art would have had very strong motivation to combine the teachings of these references.

4. Fischler's disk drive needs the VFO to implement his ZBR system. The VFO is an anticipator-synchronized phase-locked loop. Finding 15, supra. Fischler's VFO is the ZBR analog of Pederson's window generator, which is a clock-synchronized phase-locked loop. Finding 11, supra. The person having ordinary skill in the art would not have needed Pederson's window generator to implement Pederson's diagnostic system in Fischler's disk drive because Fischler has its own window generator, the VFO. Consequently, the person having ordinary skill in the art would have been motivated to build the following diagnostic circuit using the VFO:



5. The variable delay means and anticipator would be coupled in common to the same input because Pederson's detecting means compares signals from the same source. The VFO in a ZBR system uses the read data signal, not a clock signal, so the

variable delay would have to use the same signal. The detecting means would also be coupled with the VFO and the variable delay means. The PLL in Fischler's VFO corresponds to the "conventional" PLL that comprises Appellant's window generator. Moreover, Fischler's PLL is coupled in series, and synchronized, with the anticipator **62**, which Appellant has conceded corresponds to the claimed DRDSS circuit. Consequently, we conclude that the combination of Pederson and Fischler, in the manner that the references suggest, would meet the limitations in claim 12.

6. The phase shifting set forth in claim 15, which depends from claim 12, is precisely corresponds to the phase shifting caused by Pederson's variable delay circuit **22**. (7:29-8:2.) Consequently, we conclude that this function of the claimed variable delay means does not distinguish the subject matter of claim 15 from the proposed combination of Fischler and Pederson.

7. Claim 16, which depends from claim 12, requires the window pulse generating means to comprise a PLL synchronized with the DRDSS circuit. As we noted above, Fischler's VFO comprises a PLL synchronized with an anticipator that corresponds to the claimed DRDSS circuit. Consequently, this limitation does not distinguish the subject matter of claim 16 from the proposed combination of Fischler and Pederson.

8. Claim 17, which depends from claim 16, requires the PLL to include a variable oscillator generating a signal based on the zone from which data is being read (course control) and the phase difference between the signal and the DRDSS pulse (fine control). Appellant states in the specification that the operation of the PLL shown in Figure 3 is know to those having ordinary skill in the art. (Paper 1 at 14.) Consequently, we cannot conclude that this limitation distinguishes the subject matter in claim 17 from the proposed combination of Fischler and Pederson. In any case, we have already found fine control in Fischler's PLL to be equivalent. Finding 7?, supra. Claim 17 does not specify a source for the zone-based signal, so the fact that Fischler's signal comes via a digital-to-analog converter **67** instead of a microprocessor as Appellant discloses is not relevant.

9. Although we have concluded that the subject matter of claims 12 and 15-17 would have been obvious to a person having ordinary skill in the art at the time of the invention in view of Fischler and Pederson, our rationale is sufficiently distinct from the examiner's rationale that we believe due process requires a new ground of rejection pursuant to 37 CFR § 1.196(b) (Rule 196(b)).

C. Claims 13 and 14 would not have been obvious on this record

10. Claim 13 requires the detecting means to comprise

> first comparator means for comparing the data pulse delayed by said variable delay means to said window pulse, second comparator means for comparing the DRDSS-delayed data pulse to said window pulse, and third comparator means for comparing said first and second comparator means to produce an error indication if the comparison of said first comparator means differs from the comparison of said second comparator means.

11. The examiner builds on the premise that Pederson teaches a first comparator **18**. (Paper 9 at 5.) Appellant concedes that the error detector **32** of diagnostic circuitry **18** (Fig. 2) corresponds to the first comparator means. (Paper 14 at 27.) According to the final rejection (Paper 9 at 5), the combination of Pederson

> would require two additional comparators. One would compare the anticipator's delayed data pulse to the window in order to account for zonal variations. An error would occur if the two comparisons were different, so a third comparator would be needed in order to detect errors.

The examiner does not explain how the references, as understood by one having ordinary skill, would have lead to this conclusion. The answer does not defend the rationale in the final rejection, but explains that "additional comparators presented in the claim comprise duplicate components [and] that duplicating parts for a multiplied effect is not the type of innovation for which a patent monopoly is to be granted. See St. Regis Paper Co. v.

Bemis Co., Inc., 193 USPQ 8, 11." (Paper 15 at 6.) In St. Regis Paper, the Court of Appeals for the Seventh Circuit held that redundancy of layers to confer strength was obvious in the paper bag art. 549 F.2d 833, 838-39, 193 USPQ 8, 11 (7th Cir. 1977). In the present case, the comparators are not redundant since each has distinct inputs. The examiner's rationale for the rejection does not comport with the language of the claim so we reverse this rejection.

12. Claim 14 depends from, and thus incorporates the limitations of, claim 13. Consequently, we reverse the rejection of claim 14 as well.

DECISION

We affirm the rejection of claims 12 and 15-17 under section 103 in view of Pederson and Fischler, albeit under a significantly different rationale. Hence, the affirmance is a new ground of rejection pursuant to Rule 1.196(b).

We reverse the rejection of claims 13 and 14 under section 103 in view of Pederson and Fischler.

Any request for reconsideration or modification of this decision by the Board of Patent Appeals and Interferences based upon the same record must be filed within one month from the date of this decision. 37 CFR § 1.197.

Alternatively, Appellant may elect to prosecute the new grounds of rejection entered pursuant to 35 CFR § 1.196(b) by amendment or showing of facts, or both, not previously of record. 37 CFR § 1.196(b)(1). We set a shortened statutory period for making a response under this provision to expire two months from the date of this decision.

This decision is not final for purposes of review under 35 U.S.C. §§ 141 and 145. 37 CFR § 1.196(b).

Any extension of the period for taking subsequent action in this appeal will be governed by 37 CFR § 1.136(b).

AFFIRMED-IN-PART, 37 CFR § 1.196(b)

JAMES D. THOMAS Administrative Patent Judge	)	
KENNETH W. HAIRSTON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
RICHARD TORCZON Administrative Patent Judge	)	

Appeal No. 95-2218
Application 07/902,073

CURTIS, MORRIS & SAFFORD
c/o William S. Frommer
530 Fifth Avenue
New York, New York 10036